Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A multi-domain vertical alignment (MVA) LCD panel, comprising:

a first substrate having a plurality of pixel regions arranged in arrays;

a second substrate positioned parallel to and directly above the first substrate;

a plurality of common lines positioned on a surface of the first substrate facing the second substrate, each common line traversing corresponding pixel regions;

a plurality of pixel electrodes respectively positioned in each pixel region and above the common lines, each pixel electrode comprising a plurality of slits;

a dielectric layer positioned between the common lines and the pixel electrodes;

a liquid crystal layer positioned between the first substrate and the second substrate;

a common electrode layer positioned on a surface of the second substrate facing the first substrate; and

a plurality of protrusions positioned on a surface of the common electrode layer, each protrusion being arranged parallel to and alternately with each slit, the protrusions

and the common lines positioned in the pixel regions being partially overlapped.

[c2] 2. The multi-domain vertical alignment LCD panel of claim 1 further comprising a color filter layer positioned between the second substrate and the common electrode layer.

[c3] 3. The multi-domain vertical alignment LCD panel of claim 1further comprising a black matrix layer positioned on the surface of the second substrate facing the first substrate, and corresponding to areas outside of each pixel region of the first substrate.

[c4] 4. The multi-domain vertical alignment LCD panel of claim 1, wherein the common lines are electrodes of storage capacitors.

[c5] 5. The multi-domain vertical alignment LCD panel of claim 1 further comprising a plurality of thin film transistors (TFTs) positioned in each pixel region.

[c6] 6. The multi-domain vertical alignment LCD panel of claim 5 further comprising a plurality of data lines electrically connected to a source of each thin film transistor.

[c7] 7. The multi-domain vertical alignment LCD panel of claim 6, wherein the common lines serve as dummy cir-

cuits while the data lines are disconnected.

[c8] 8. The multi-domain vertical alignment LCD panel of claim 1, wherein critical dimensions of the protrusions are less than those of the common lines.

[c9] 9. The multi-domain vertical alignment LCD panel of claim 1, wherein each common line in each pixel region forms an H-shaped electrode pattern comprising a first electrode pattern and two second electrode patterns, the first electrode pattern traversing a middle of each pixel region, and the two second electrode pattern being perpendicular to the first electrode pattern.

[c10] 10. A multi-domain vertical alignment (MVA) LCD panel, comprising:

a first substrate having a plurality of pixel regions arranged in arrays;

a second substrate positioned parallel to and directly above the first substrate;

a plurality of electrode patterns respectively positioned in each pixel region, each electrode pattern being H-shaped and comprising a first electrode pattern traversing a middle of each pixel region, and two second electrode patterns perpendicular to the first electrode pattern;

a plurality of pixel electrodes respectively positioned in

each pixel region and above the electrode patterns, each pixel electrode comprising a plurality of slits not overlapping the first electrode pattern;
a dielectric layer positioned between the common lines and the pixel electrodes;
a liquid crystal layer positioned between the first substrate and the second substrate;
a common electrode layer positioned on a surface of the second substrate facing the first substrate; and
a plurality of protrusions positioned on a surface of the common electrode layer, each protrusion being arranged parallel to and alternately with each slit, the protrusions and each first electrode pattern being overlapped.

[c11] 11. The multi-domain vertical alignment LCD panel of claim 10 further comprising a color filter layer positioned between the second substrate and the common electrode layer.

[c12] 12. The multi-domain vertical alignment LCD panel of claim 10 further comprising a black matrix layer positioned on the surface of the second substrate facing the first substrate, and corresponding to areas outside of each pixel region of the first substrate.

[c13] 13. The multi-domain vertical alignment LCD panel of claim 10, wherein the electrode patterns are electrodes

of storage capacitors.

[c14] 14. The multi-domain vertical alignment LCD panel of claim 10, wherein the electrode patterns are electrically connected to one another.

[c15] 15. The multi-domain vertical alignment LCD panel of claim 10 further comprising a plurality of thin film transistor (TFTs) respectively positioned in each pixel region, and a plurality of data lines respectively electrically connected to a source of each thin film transistor.

[c16] 16. The multi-domain vertical alignment LCD panel of claim 15, wherein the electrode patterns serve as dummy circuits while the data lines are disconnected.

[c17] 17. The multi-domain vertical alignment LCD panel of claim 10, wherein critical dimensions of the protrusions are less than those of the electrode patterns.